What is claimed is:

1. A data sequence conversion circuit which takes as an input any one of a plurality of input data sequences having different data widths, and which converts said input data sequence into an output data sequence having a prescribed data width for output, said circuit comprising:

a first parallel shift register for holding said input data sequence;

a switch matrix for taking the data held in said first parallel shift register as input data, and for outputting said input data in a distributed fashion in accordance with a rule selected by a control signal from a plurality of predetermined rules; and

a second parallel shift register for taking the data output from said switch matrix as input data, and for outputting said input data as a data sequence having said prescribed data width.

2. A data sequence conversion circuit as claimed in claim 1, wherein when the data widths of said plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of said output data sequence by Wo, said first parallel shift register has a data width at least equal to the largest value of Wn (n = 1, 2, 3, ...), and has the number of stages at least equal to the largest value of the quotients QIn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn (n = 1, 2, 3, ...) and Wo by Wn.

3. A data sequence conversion circuit as claimed in claim 1, wherein when the data widths of said plurality of input data sequences are denoted by Wn (n = 1, 2, 3, ...), respectively, and the data width of said output data sequence by Wo, said second parallel shift register has the number of stages at least equal to the largest value of the quotients QOn (n = 1, 2, 3, ...) each obtained by dividing the least common multiple of Wn

(n = 1, 2, 3, ...) and Wo by Wo.

4. A data sequence conversion circuit as claimed in claim 1, wherein the data widths of said plurality of input data sequences are 5 bits, 4 bits, and 3 bits, respectively, the data width of said output data sequence is 8 bits, said first parallel shift register has a 5-bit data width and eight stages, and said second parallel shift register has five stages.

5. A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, said switch matrix outputs said input data so that Wn×QIn units of data input and held in the first stage to the (QIn)th stage in said first parallel shift register as counted from the input side thereof are input to the first stage to the (QOn)th stage in said second parallel shift register as counted from the output side thereof, where QIn is the quotient of the least common multiple of Wn and Wo divided by Wn, and QOn is the quotient of the least common multiple of Wn and Wo divided by Wo.

6. A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, the shift clock frequency Fi of said first parallel shift register and the shift clock frequency Fo of said second parallel shift register have a relation defined by Fi/Fo = Wo/Wn.

7. A data sequence conversion circuit as claimed in claim 1, wherein when the data width of said input data sequence is denoted by Wn, and the data width of said output data sequence by Wo, each time QIn data sequences are input into said first parallel shift register, Wn×QIn units of data are input into said second parallel shift register via said switch matrix, following which QOn data sequences are output from said second

parallel shift register.

8. A printer comprising a data sequence conversion circuit as claimed in claim 1, said data sequence circuit being located between a jaggy correction circuit and a line-like printhead.